DIGITAL DISPLAY FOR THE KW-2000B TRANSCEIVER

AN UPDATE FOR A FINE OLD RIG

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IN the face of ever-increasing transceiver prices, the prospect of upgrading older equipment becomes increasingly attractive. A popular example of such a piece of equipment is the KW-2000B, offering 5-band coverage, SSB/CW, with an input power of 180 watts p.e.p., usually available at a fraction of the price of its present day counterparts. A comparatively simple transceiver such as the '2000B lends itself to modification (for example, *see* "Modifying the KW-2000A Transceiver for the 10 MHz", *Short Wave Magazine*, May 1982).

One feature the author has found very annoying with the rig is the inaccuracy of the analogue dial, it being very diffficult to net precisely on any specific frequency. The addition of a digital readout would enable an accurate check on frequency (and also show just how much the VFO drifts during operation . . .), allowing very accurate netting.

A study of the various mixing processes carried out in the KW reveals that the VFO tunes from 2.5-2.7 MHz, producing a 200 kHz allocation for each master oscillator crystal. The output from the VFO is mixed with 455 kHz SSB to produce a variable IF of 2.955-3.155 MHz. This signal is subtractively mixed with a crystal master oscillator to produce RF in the appropriate amateur band. A consequence of this mixing process is that as the transceiver is tuning to a higher frequency, the VFO frequency is in fact decreasing. Hence any digital readout must read '200 kHz' when the VFO is at 2.5 MHz, falling to '0 kHz' when a frequency of 2.7 MHz is attained.

Operation

The basic operation of the display is probably best described with the aid of Fig. 1, a simplified block diagram. All clock pulses are derived from a 2.7 MHz crystal oscillator, applied to input A, the sinewave output from the VFO being squared off and applied to input B. These two signals pass to the clock and data inputs, respectively, of a D-type bistable, forming a digital subtractive mixer. When the VFO is tuned to 2.5 MHz, a frequency of 200 kHz is produced at the Q output, falling to 0 kHz as the VFO frequency rises to 2.7 MHz, in accordance with the requirement illustrated in the previous paragraph. Additionally, the 2.7 MHz signal undergoes a division of 27,000 to generate 100 Hz clock for timing purposes. A further division by 2 is implemented to generate 50 Hz pulses, connected to the display enable input (DEI) of the counter/display module. Whenever this input goes high, the data stored in the counters is applied to the 4-digit, 7-segment, display; hence in this application the display will be on for 10mS, followed by a 10mS off, or blanking period. It is during this period that counting must occur (otherwise the display will be a meaningless jumble of figures), and this is achieved by allowing the clock inhibit pin of the counter/display module to go low during an appropriate period of blanking. The interval between counting periods is determined by the action of the ripple counter, in conjunction with the count interval controller (another D-type bistable).

Assume that the ripple counter has just been reset to zero. It will count up in binary upon receiving 50 Hz clock pulses from the divider chain. For the time interval that the output Q4 is low, the data input of the count interval controller will be held low, as will the Q output irrespective of 100 Hz clock pulses being applied to the clock input. However, once 2^3 clock pulses have been received, Q4 goes high. When the next clock pulse is applied to the controller, Q goes high, causing the clock inhibit input to go low, allowing 10mS-worth of pulses from the subtractive mixer to reach the counters. At the same time, the ripple counter is reset to zero, causing Q4 to go low. On receiving its next clock pulse, the Q of the controller goes low, and so the process continues. . . . It will also been noted that as Q4 goes high it opens the way for a 0.1mS reset pulse immediately proceeding a count period, resetting the count to zero.

This control logic at first may seem unnecessary as it would appear much easier to count during all blanking periods. This

Table of Values
Fig. 2

R1, R2	TC1 = 3-30 pF
R4, R15 = 10K	Q1, Q2 = BC109
R3 = 4M7	D1, D2, D3 = 1N4148
R5 to R13,	IC1 = 4069
R17 = 100K	IC2 to IC6 = 4017
R14 = 47K	IC7, IC8 = 4013
R16 = 1K	IC9 = 4040
C1 = 100 pF	IC10 to IC13 = 4026
C2 = 1 nF	Xtal = 2.7 MHz
C3 = 100 nF	LED Display = four 7-segment common cathode.
C4 = 100 μF	

Note: For IC1, 7, 8, +8V to pin 14, OV to pin 7; all other IC's, +8V to pin 16, OV to pin 8.

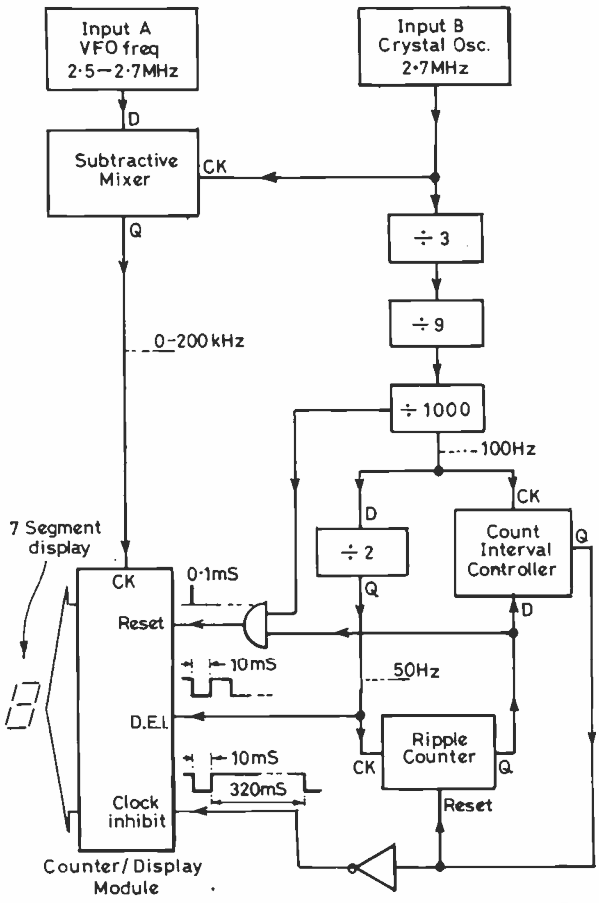


Fig.1 SIMPLIFIED BLOCK DIAGRAM OF THE KW-2000B DIGITAL DISPLAY

E 169

View of the modified front panel.

method was originally adopted by the author, but an intolerable amount of jitter occurred due to the 100 Hz (least significant) digit changing alternately between two digits, this change taking place at any frequency from 0 to 50 Hz. With the circuit as shown (Fig. 2), the count rate is one count every 320mS, which is the best compromise between annoying jitter and sluggish tracking of the

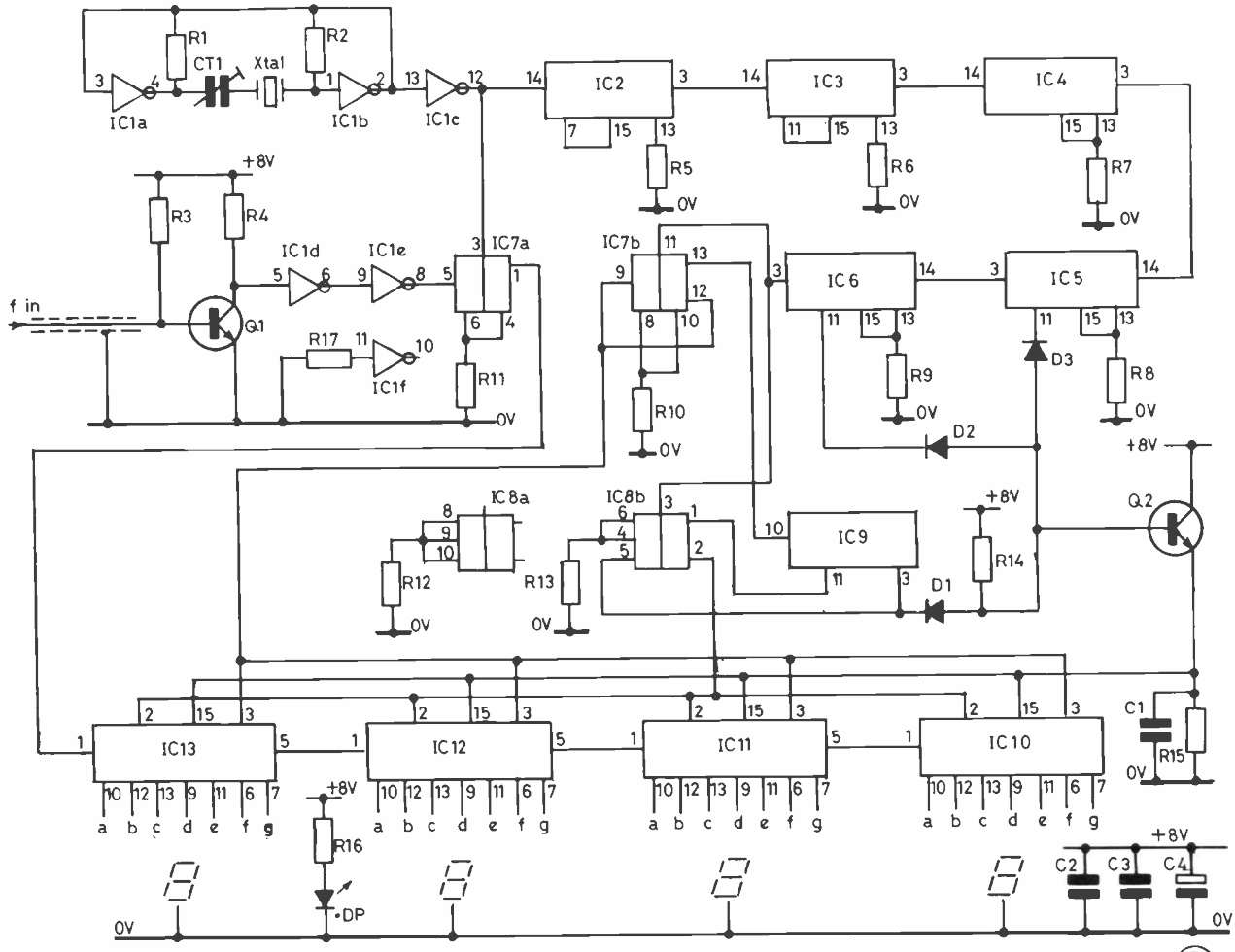


Fig. 2 KW-2000B DIGITAL DISPLAY CIRCUIT DIAGRAM

E 170

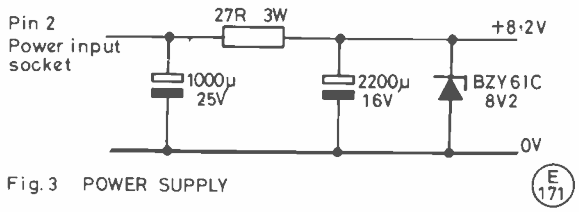


Fig. 3 POWER SUPPLY

VFO during tuning. For a faster count rate of 160mS, the data input of the controller should be connected to Q3 of the ripple counter, a 640mS rate is available by connection to Q5, etc., etc. . . .

The 2.7 MHz crystal and associated inverters present fast squarewaves to the divider chain, comprising of IC2 (divide by 3), IC3 (divide by 9), followed by IC4, 5, 6 — all decade dividers. The resultant 100 Hz squarewave undergoes a further stage of division by 2, IC7*b* thereby supplying display enable pulses to the counter/display module, IC10, 11, 12, 13. IC7*a* forms the subtractive mixer, being fed with 2.7 MHz clock pulses and a squarewave representation of the VFO frequency (produced by Q1 and two associated inverters), the mixer output being applied to the input of the counter/display module. The ripple counter, IC9, is fed with 50 Hz clock pulses and is controlled by IC8*b*, the count interval controller, applying clock inhibit pulses to the counter/display module. D1-4, Q2 and associated circuitry forms a 3-input AND gate and is used to control reset pulses to the counters. It will be seen that a positive potential (supplied *via* R14), will only be present when all of the diodes are reverse biased, *i.e.* when pin 11 IC6, pin 11 IC5, pin 3 IC5, are all high. This will only occur during the 0.1mS period before any count period. During this period, Q2 conducts and a high pulse resets the counters.

Fig. 3 shows a suitable power supply for the display, power being drawn from the + 12V DC available within the rig, used for relay switching.

Modifications

See photographs. The prototype unit was constructed on *Veroboard* (using IC sockets and usual CMOS precautions), and mounted in a small aluminium box 100 x 100 x 30mm. in dimensions, in turn mounted on three, 50mm. standoffs above the Tx/Rx relays. The original analogue dial was removed and a 4-digit, 7-segment, LED display mounted on *Veroboard* and slotted in front of the VFO box was added. To create a more 'professional' look, the perspex window was removed and a grey border (surrounding the display) was added using aerosol spray paint.

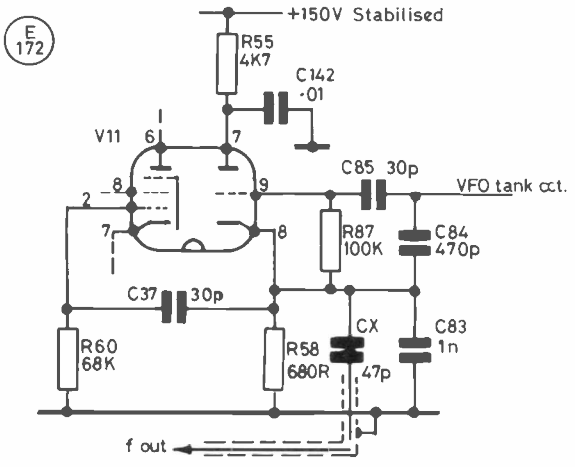
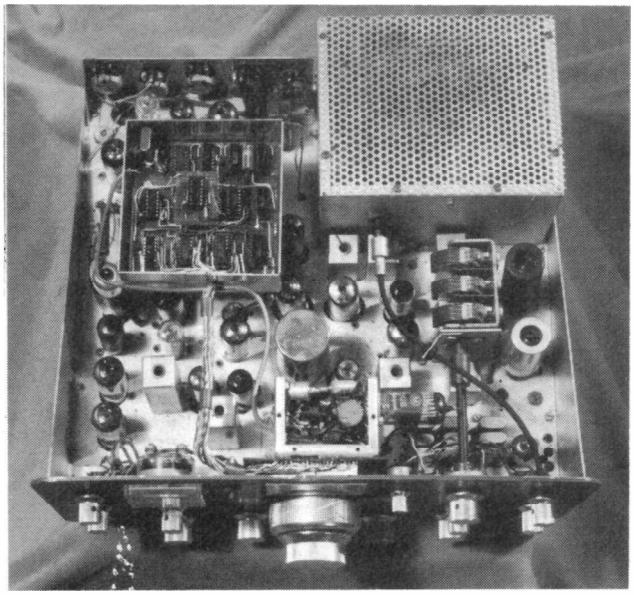
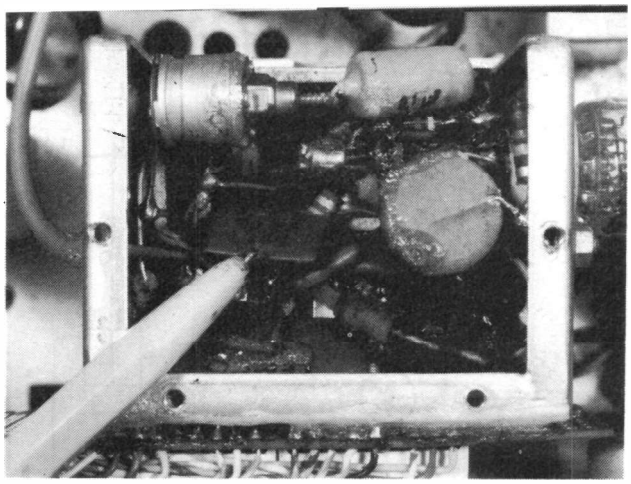


Fig.4 VFO RF PICK-UP





Above, general layout of G4NCA's prototype. Below, details of inside the VFO box showing the addition of Cx. (In the prototype, as a 47pF capacitor was not to hand, a 56pF was connected in series with a 470pF).

Fig. 4 details how RF pickup from the VFO was derived. Initially RF pickup was achieved from the buffered output from the VFO box; this arrangement worked fine on receive, but a 'scope placed at this point during transmit revealed a multitude of frequencies due to the action of close-coupling with the balanced mixer, V4. The addition of Cx (47pF silver mica) into the VFO proved to have not detrimental effects. Removal of the top of the VFO reveals a convenient free tag on which to mount Cx, and a small hole drilled in the side of the VFO box is used to pass the miniature co-ax. *Bostik*, or a similar adhesive, is used to secure the capacitor and other wiring from the effects of vibration.

Conclusion

The display has been in use at the author's QTH for several months, proving to be invaluable for netting and providing a very economical solution to the problem (the prototype was constructed for less than £15 inclusive). The use of a screened housing eliminated all the usual 'nasties', none being detected whilst running the rig into a dummy load.