DIGITALISATION OF THE KW-2000B TRANSCEIVER, PHASE II

A SIMPLE ADD-ON VFO STABILISER TO COMPLEMENT THE DIGITAL DISPLAY DESCRIBED IN LAST MONTH'S ISSUE

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ONE of the fascinating aspects of modernising older equipment (or for that matter, prototype construction) is that no sooner has a problem been identified, solutions found and modifications completed, than attention is brought (as a result of the initial modification) to other, often more subtle, shortcomings within the equipment. A consequence of this is that a continuous process is set up of successive modifications, with (hopefully) an end product that performs exactly to the individual's wishes. This approach is undoubtedly the best for home construction, ensuring that individual circuit elements do in fact work before stringing them all together. There is nothing more frustrating, having neatly built a large project, than turning on to find nothing happens (and even worse, seeing it go up in smoke!), to be faced with the prospect of breaking it down to fault-find. It was for this reason that the above title was chosen, this unit being the second modification undertaken on the 'old faithful' KW-2000B.

Having constructed a digital frequency display for the KW-2000B, it rapidly became apparent just how much the VFO drifts from initial turn-on, and indeed for several hours after. When using the rig for CW or SSB contacts this drift is quite tolerable, simply necessitating a slight tweak of the tuning every now and again. However for the more frequency 'sensitive' modes such as RTTY or SSTV the problem becomes more acute; for instance, in the author's case, obtaining reliable copy from the Sunday morning GB2ATG RTTY broadcasts on 80m. would involve tracking the VFO throughout the transmission. Additionally, this inherent drift proves to be very annoying for the distant receive station during transmission, in turn having to track his/her VFO, often resulting in the QSO wandering up and down the band at an alarming rate.

As much of the work in producing some type of digital stablisation unit had already been undertaken with the construction of the digital display, a simple add-on unit became a very attractive solution to the problem.

Within the VFO tank circuit of the '2000B there are (very conveniently) two DC controlled varicap diode branches; one of which is used in the IRT circuitry, the other involved in the calibration adjustment of the now obsolescent analogue dial. Use is made of this in the stabliser circuitry, enabling any offset frequency to compensate for drift to be created by a small change in the steady reverse bias DC voltage across the varicap diode. An increase in this voltage will reduce the capacitive effect of the diode and cause the frequency to rise. Correspondingly, a reduction in voltage will increase the capacitive effect and the frequency will fall.

Operation

The basic outline of the system is shown in Fig. 1, all power, control and timing signals being derived from the digital display board. Input pulses, supplied by the subtractive mixer (IC7) in the display board are applied to the clock input of the BCD counter, IC14. The signal applied to the clock enable input of the counter is, in fact, exactly that applied to the counters in the display board.

Tables of Values

Fig. 2

R18 to R21, R23 to R25 = 47K
R22 = 1M
R26, R27 = 1K
R28 = 470K
C5 = 100 µF
C6 = 1000 µF
C7 = 220 µF, 12V elec.
C8 = 100 nF polyester
IC14 = 4518
IC15 = 4042
IC16 = 4063
IC17 = 4081
Q3, Q4 = BC109
Q5 = BC212
D4, D5 = 0.2-in. LED

Note: capacitors C5, C6 should be preferably low-leakage types, such as tantalum 10V working.

Fig. 4

RA, RC = 10K
RB, RE = 3K3
RVD = 1K linear

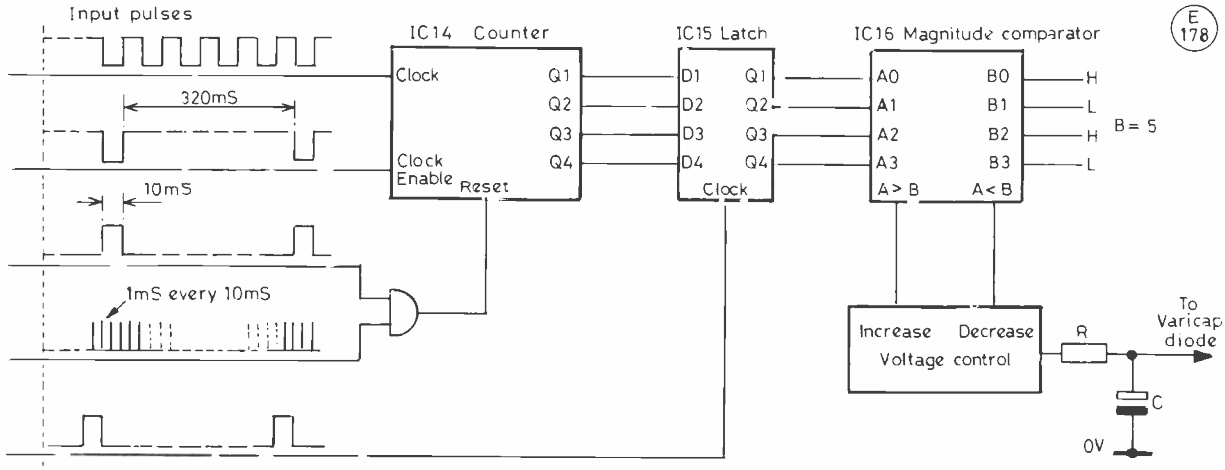


Fig. 1 BLOCK DIAGRAM

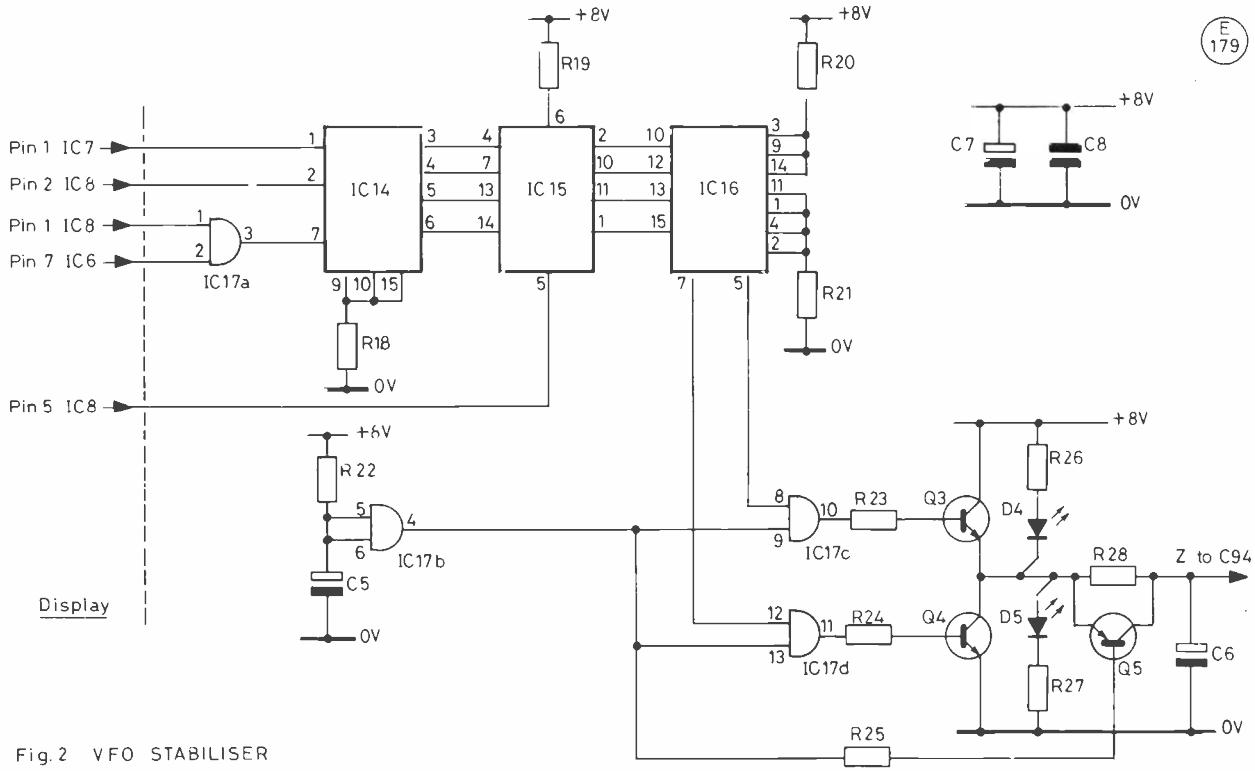


Fig. 2 VFO STABILISER

In this case however, as this signal is connected to the clock enable input (as distinct from the clock inhibit input), the count will be for 320mS, followed by a 10mS inhibit period. As the count is operational for approximately ⅓-second, the output from the counter will consist of the four least significant bits representing the frequency in 3 Hz steps. during the 10mS inhibit period the count is applied to the latch, IC15, and the counter is subsequently reset in anticipation of the next count period. The output of the latch is applied to the 'A' input of IC16, a 4-bit magnitude comparator; the 'B' input is set to denary 5 (0101 in binary). Two

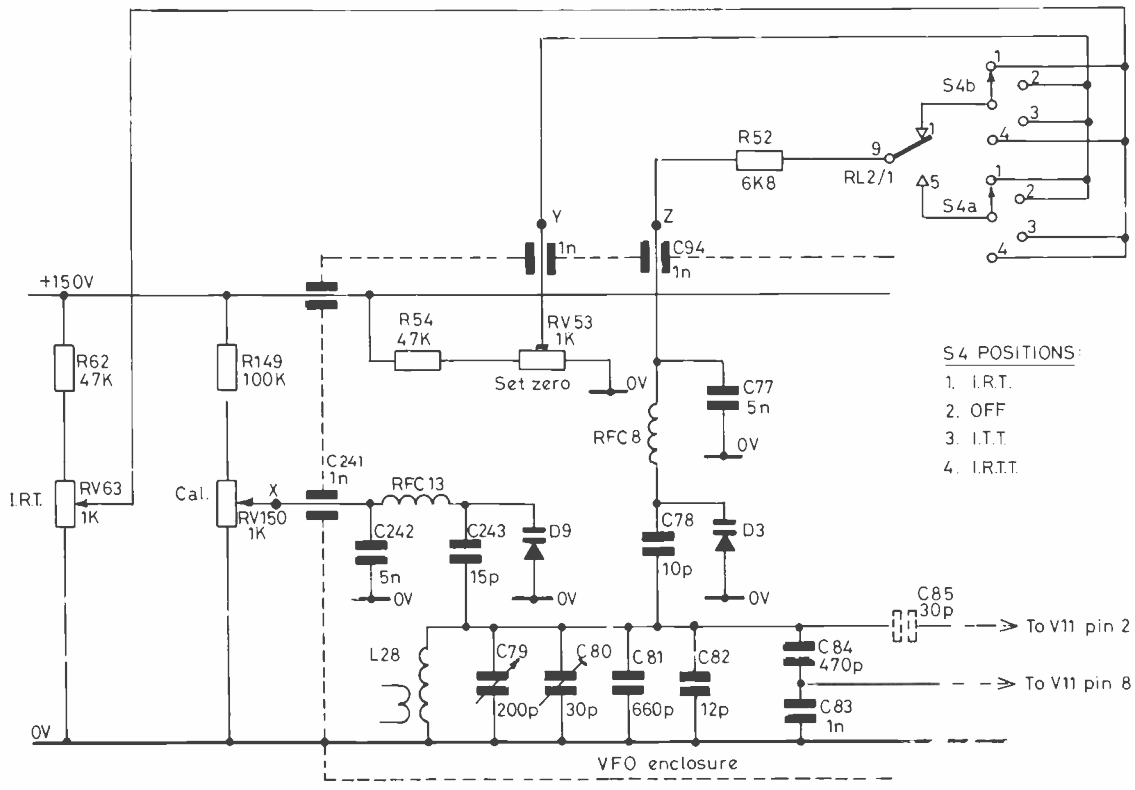
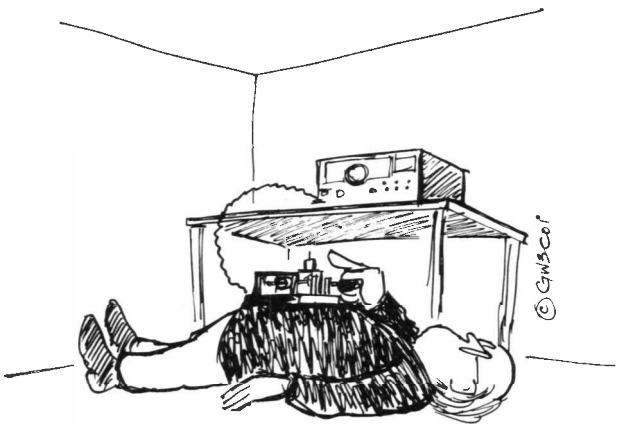


Fig. 3 KW2000B EXISTING I.R.T. CIRCUIT

out of the three outputs from the comparator are used, A>B which will go high when the magnitude of input 'A' is from 6 to 9 and A<B, which will go high when the magnitude of 'A' is less than that of 'B', *i.e.* from 0 to 4. These outputs are fed to the voltage control unit, which applies a voltage (*via* the high resistance resistor, R) to the capacitor C and the varicap diode within the VFO tank circuit. The voltage control unit will increase the voltage across C when A>B, maintain a constant voltage when A = B and decrease the voltage on the capacitor when A<B. The rate of change of voltage is controlled by the values of R and C and the time constant was found to be fairly critical in the author's unit for smooth operation of the stabiliser, although a large range of values was tried and gave satisfactory results.

If either R or C are of too small a value, a noticeable 'warbling tone' is produced due to rapid changes in the value of voltage as the stabiliser overshoots its locking point. Conversely, if R and C are of too large a value, the stabiliser will not be able to cope with the large frequency drifts occurring soon after turn-on and lock will be lost. The locking point exists when the condition A = B = 5 occurs within the magnitude comparator, at which point a constant voltage will be present on the varicap diode. The locking points occur at approximately 33 Hz steps, once the tuning is set onto a specific frequency, and the unit will lock to the nearest step and remain there until the tuning is again adjusted. Assume that the VFO drifts slightly high of the locking point (*i.e.* by more than 3 Hz): as the VFO frequency rises, the output from the subtractive mixer will fall, in turn causing the magnitude of 'A' to fall. A<B will go high, decreasing the voltage on the varicap, increasing the effective capacitance in the tank circuit and lowering the VFO frequency. This action will take place until the condition A = B = 5 is attained, upon which the voltage once again returns to a constant value. Using this method of locking, drifts in either direction can be catered for, enabling even the most stubborn of oscillators to be 'tamed' easily.

Fig. 2 details the schematic diagram of the unit. The operation follows that of the block diagram but with one important additional facility. For the effective operation of the unit it is essential that the capacitor C (C6 in Fig. 2) is charged to its steady state value (in the case of this unit, 4 volts) before any attempt at stabilisation is made; failure to do this will result in the capacitor being only partially charged on the formation of the first locking point, and if a positive VFO drift occurs (causing A<B) then the amount by which the capacitor can discharge will be severely limited — in turn limiting the amount of stabilisation possible.



"I picked up this tummy bug at a recent rally. . . ."

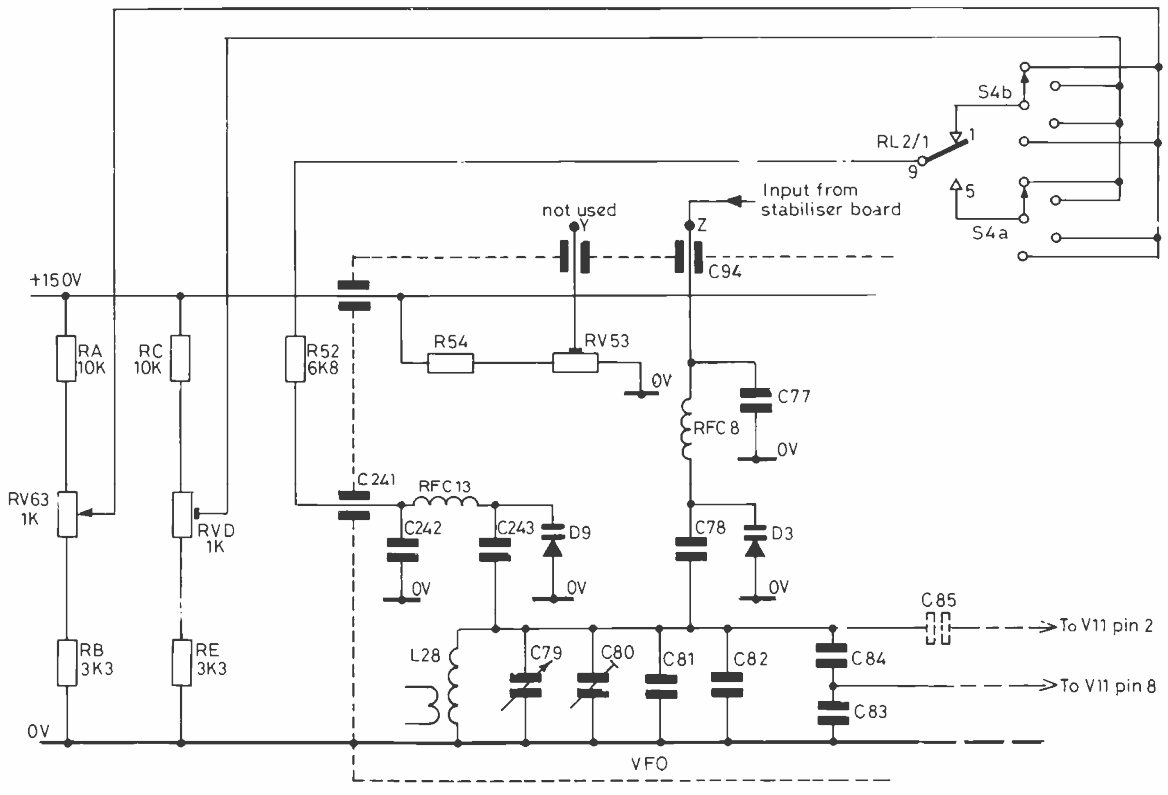


Fig. 4 MODIFIED I.R.T. CIRCUIT

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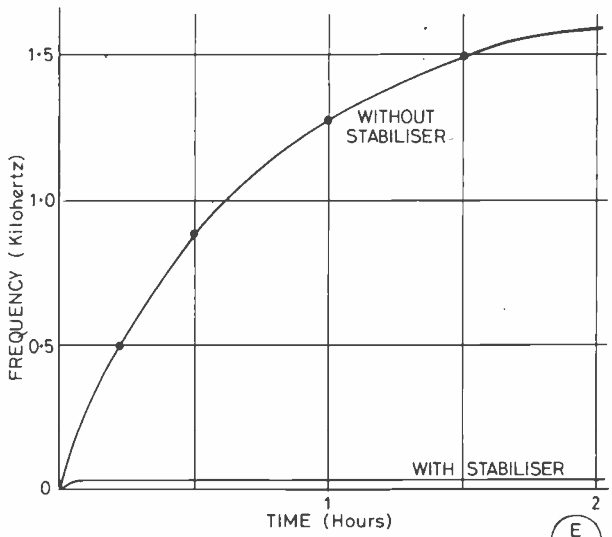

Fig. 5 RELATIVE DRIFT vs TIME

Conclusion

The improvement in stabilisation is best illustrated with the aid of Fig. 5, graphically showing drift of the VFO with and without stabilisation, relative to the frequency at transceiver turn-on (valves having warmed up of course!). In both cases the drift was measured at an initial frequency of 2.600 MHz, at an ambient temperature of 15°C, ensuring similar heating cycles. Operation of the transceiver is made much simpler, frequency stability being in the order of that given by most present day synthesised transceivers — admittedly without some of the facilities of the modern 'Far East wonders', but then again at a fraction of the cost.

Undoubtedly, within a few weeks the lid will be off the rig again as yet another mod. is performed — in fact the author has already some ideas on improving sensitivity on the higher frequency bands; well, fingers crossed. . . .

It is also pointless attempting to stabilise the VFO frequency immediately following turn-on, as drift during the first minute or so is inevitable in any valve equipment. Both the initial charging circuit and stabilisation inhibit circuits are controlled by the one-shot monostable consisting of R22, C5 and IC17*b*. When the supply voltage is connected, C5 charges *via* R22, causing a low output from the gate IC17*b* until a threshold voltage is reached, upon which the output goes high. The delay produced by the circuit is in the region of two minutes, after which control signals are extended *via* IC17*c-d* to the voltage controller transistors Q3 and Q4; if neither Q3 or Q4 are conducting, a voltage of 4V will be present at point 'M' and both LEDs will glow dimly. If Q3 is conducting, a voltage of approximately 8V will be present at 'M' and D5 will glow brightly, indicating a charge condition. Similarly, when Q4 conducts, a voltage of approximately 0V will be present at 'M' and D4 will be illuminated, indicating the discharge (or A<B) condition. From the table of values, it can be seen that R28 (shown as R in Fig. 1) and C6 (C in Fig. 1) are of comparatively large value. To effectively charge C6 to the 4V value was found to take around 10 minutes; obviously this time interval is excessive. The addition of R25 and Q5 will effectively short-circuit R28 for the duration that the output of IC17*b* is at logic 0, becoming a virtual infinite resistance as soon as the output flips to the '1' state. In this way, very effective initial turn on charging occurs, whilst maintaining a sufficiently high R, C time constant.

Modifications

Figs. 3 and 4 detail the relevant parts of the VFO circuitry before and after modification, points 'X' (connected to purple wire), 'Y' (blue wire) and 'Z' (yellow wire) being connections to feedthrough capacitors on the bottom of the VFO enclosure. Note that the roles of the varicap diode branches are in fact reversed; that is, the one which was used for the IRT circuitry before modification is now used for the stabiliser, the diode branch previously used in the calibrate circuitry now being used for the IRT. The addition of the four resistors, RA to RE, will reduce the effective spread of the IRT control from ±6 kHz (which the author found very awkward — requiring 'safe cracker' fingers to net precisely on frequency) to a less daunting ±600 Hz. The complete stabiliser should be placed in a screened box (in the same box as the display unit if possible), with D4 and D5 mounted in the lid of the box so that operation of the stabliser may be readily checked.

Comtech **announce the introduction of the new DB-1 series of desk microphones. Features include a wide range of inserts of various impedances, p-t-t or on-off switching, and models are available with integral microphone pre-amplifiers or line amplifiers, 'busy' signal lights and 'time-out' timers. For full details contact R. L. Glaisher,** *Communication Technology Ltd.*, **279 Addiscombe Road, Croydon CR0 7HY. Tel: 01-656 3631. Telex: 269738.**